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Domino Logic-Based Full Adder for Power Efficient VLSI Applications

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Abstract-**This research analyses a full adder circuit realized by implementing domino logic. Dynamic logic style domino logic has greater speed and power efficiency in comparison to static CMOS logic. In the proposed design of a full adder, inherent characteristics of domino logic such as dynamic node precharging and low static power consumption contribute to great performance metrics. The design and implementation of a domino-based full adder, along with simulation and performance evaluation, are covered in detail. The performance parameters, including propagation delay, power consumption, and area, are examined through extensive simulations with industry-standard DSCH and Micro wind tools. These results are compared with a conventional CMOS-based full adder to highlight the improvements that the domino logic approach brings in.**

Keywords— CMOS, Domino, Full adder, Performance Parameters.

Introduction

Transistor density is rising quickly every day in the rapidly expanding VLSI industry. Moore's law states that transistor density doubles on its own every 18 months. The device's area, latency, and power consumption will all rise in tandem with the number of transistors. Therefore, a technology that can decrease the area and improve the device's performance is needed. The semiconductor industry has been creating devices using CMOS technology for the past few decades, but as the number of transistors increases, so do the device's area and latency. Therefore, it is necessary to convert to a technology that has a lower latency and uses less space.

The p-MOS and n-MOS transistors are used in CMOS circuitry to create pull-up and pull-down switches. This topology facilitates quick logic execution by turning on p-MOS and charging the output to Vdd when the input is low and turning on n-MOS and providing a channel to ground when the input is high. Because of the complementary structure of the transistors—one is ON and the other is OFF—CMOS logic Favors additional benefits like extremely high noise immunity and low power consumption. However, its drawbacks include a comparatively poor operating speed and a considerable size need for complex circuits. Because of this, there is an alternate technology that has fewer transistors but faster operating speeds.

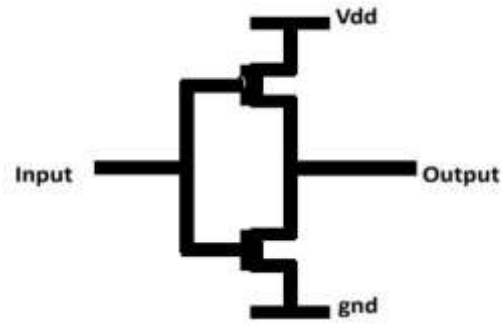

Fig 1. CMOS Logic inverter

Domino logic, a CMOS dynamic logic derivative, is perfect for digital signal processors, dynamic memory, and microprocessors since it can operate at high speeds and has less transistors. Domino logic produces high-performance devices using fewer transistors than traditional CMOS logic. A problem with cascading gates in dynamic logic is addressed by this logic technique. Domino logic gets around this problem by adding a static inverter in between stages. Domino logic's main benefits are its small size, low parasitic capacitance, and ability to operate at high speeds. Output without glitches since each gate only passes through one transition every cycle All things considered, Domino logic offers a better

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method of dynamic logic with increased effectiveness and performance.

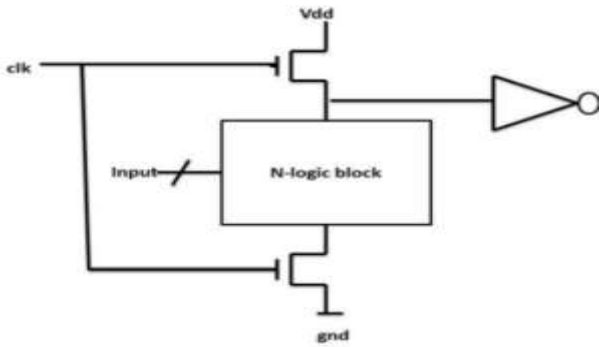

Fig 2. Domino logic

Domino Logic is a dynamic logic family used in digital circuit design, often combined with CMOS technology. It operates in two phases: Precharge When the clock signal is low, the pMOS transistor turns on, connecting the output node to the positive power supply. This precharges the output node to a logical HIGH state, ensuring a known state before evaluation. Evaluation When the clock signal goes high, the pMOS transistor turns off, isolating the output node from Vdd. If a conductive path exists from the output node to ground through the pull-down network (PDN), the output node discharges to GND, resulting in a logical LOW. If no conductive path exists, the output node remains HIGH. The circuit's output is determined by the input configuration during the evaluation phase.

Designing Techniques

The examination of a full-adder circuit will employ two design approaches, namely domino-based logic and CMOS-based logic style, and compare the outcomes. A digital circuit used to execute numerical addition is called an adder. Adders are utilized in arithmetic and logic units in calculators and computers. Three one-bit inputs, A, B, and C, are required by this combinational circuit. As illustrated in Fig., it has two outputs, the sum and the carry.

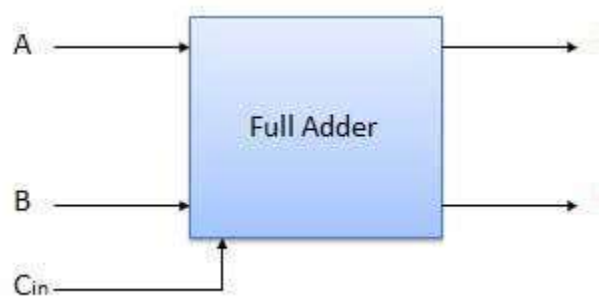

Fig 3. Block diagram of one-bit full adder

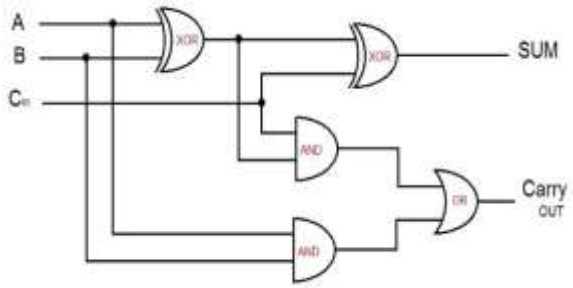

Fig 4. Logic diagram of one-bit full adder

The one-bit complete adder's gate level logical diagram, which employs two X-OR gates for sum, two AND gates, and one OR gate for carry, is displayed in Fig. The carry of a one-bit complete adder is provided by the OR gate's output, which uses the output of the two AND gates as an input. The truth table for a complete adder with CMOS-based logic is displayed in the table 1.

Inputs			Outputs	
A	B	C_{in}	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 1. Full Adder Truth Table

1. Designing of one-bit full adder based on CMOS logic - The one-bit full adder design Fig 5. shows the schematic of a one-bit full adder that uses CMOS logic. 14 p-MOS transistors are used in this circuit to charge the output capacitance, and 14 n-MOS transistors are used to discharge the output node based on the input value. Therefore, a one-bit complete adder that employs the CMOS logic type is designed using a total

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of 28 transistors. One-bit full adders are extremely complex and challenging to design since they need a lot of transistors. As shown in the figure, a significant amount of delay is introduced into the circuit by the numerous wires needed to connect the transistors.

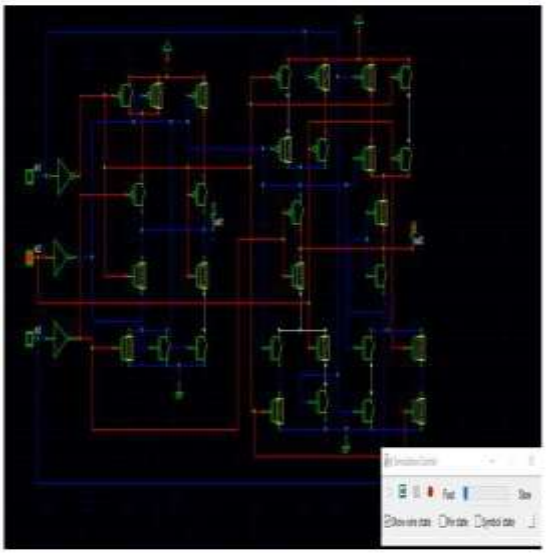

Fig 5. Schematic structure of one-bit full adder which uses the CMOS logic

2. Designing of one-bit full adder using Domino logic - The one-bit full adder design Fig6. displays the Domino logic one-bit full adder schematic. We used p-MOS transistors for the pre-charge phase an inverter and n-MOS transistors for the evaluation phase while developing the one-bit complete adder using domino logic. We have employed 16 n-MOS transistors and 4 p-MOS transistors in this logic architecture. In order to create the adder circuit using Domino logic, a total of 20 transistors are used.

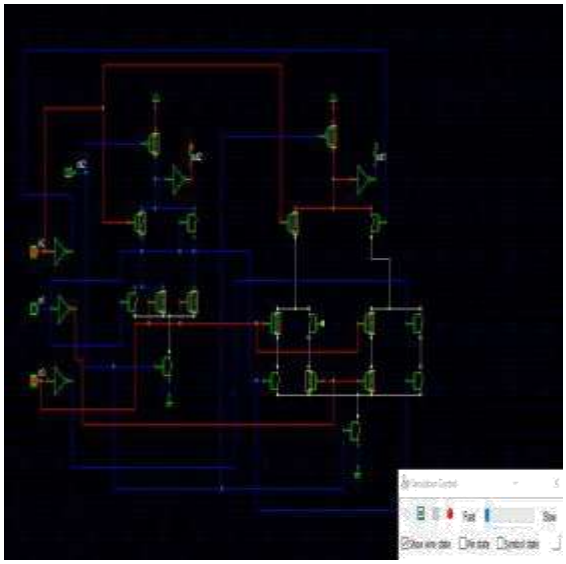

Fig 6. Schematic design of one-bit full adder which uses Domino logic

One- Bit Full Adder: Results, Discussion and Analysis

Analysis of one-bit full adder using CMOS logic:

The schematic circuit depicted in Fig 8. analyses a full adder using CMOS logic, and the findings were confirmed using the full adder truth table. Fig. displays the transient analysis result of the whole adder circuit that validates the truth table. The truth table of the whole adder circuit gate has been confirmed, as seen in Fig. When there are an odd number of high states in the input, the output "SUM" is high; otherwise, it is low. Similarly, when two or more input states are high, the output "CARRY" is high. We computed the circuit delay and power analysis waveform, which is displayed in Fig. after obtaining the precise result.

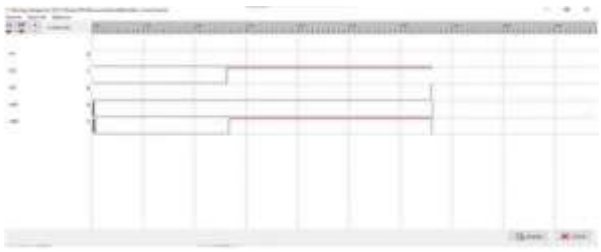

Fig 7. Timing diagram of CMOS logic

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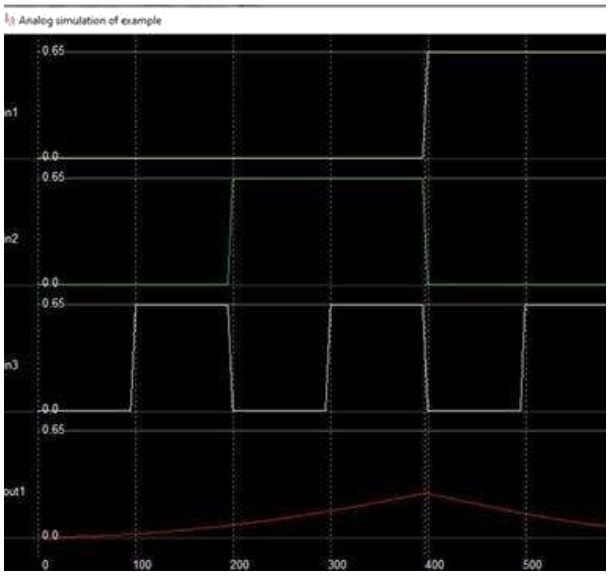

Fig 8. Simulated result of one-bit full adder based on CMOS Logic

Analysis of one -bit full adder using Domino logic:

Using Domino logic, we examined the schematic of a one-bit complete adder circuit. The outcome of this logic was then confirmed using the whole adder circuit truth table, which is displayed in Fig 9. When the clk signal is low, p-MOS will be on and charge the output node to Vdd, giving us a high output at this point. However, we utilize an inverter to obtain the adder's output, so it will display both sum and carry low.

The duration of the clk provided during the simulation will determine when the pre-charge and evaluation phases take place. Fig. displays the power analysis waveform for an adder based on Domino logic. As can be seen in Table, when creating a one-bit full adder circuit with domino logic, fewer transistors are used and there is less latency than when using CMOS logic. Domino logic saves chip space proportionately since it uses fewer transistors.

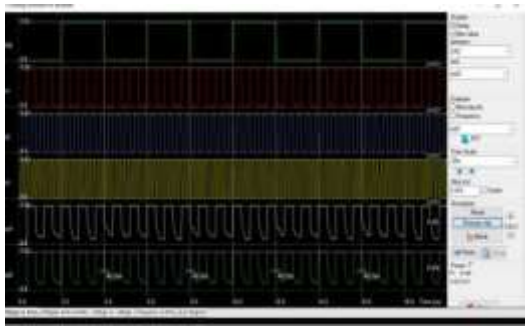

Fig 9. Simulated result of one- bit full adder using Domino logic

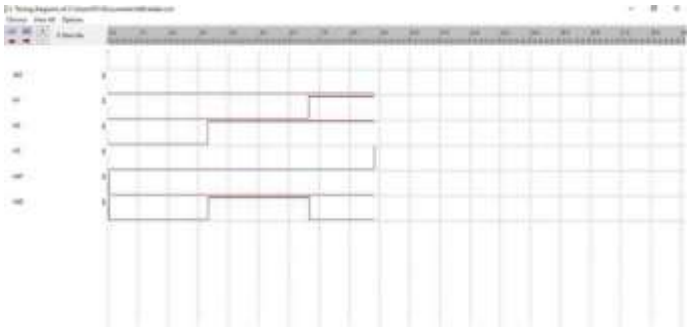

Fig 10. Timing waveform of Domino logic

The chip area has been reduced by over 28.5%. This is an estimate since we have less p-MOS transistors (manufactured in n-well), which means that more chip space can be conserved. Both logics' delays have been computed and are shown in the table. This table suggests that, in comparison to CMOS logic, Domino logic exhibits a 47.36% lower delay. Figures 7 and 10 illustrate the timing waveforms on CMOS and Domino Logic.

Conclusion

The design and analysis of a complete adder circuit utilizing Domino and CMOS logic are presented in this study. Our findings, using 45nm technology and DSCH and Micro Wind software, demonstrate that Domino logic performs better than CMOS logic in a number of important areas. Domino logic specifically exhibits: Greater accuracy, fewer transistors, less delay, less chip size, and lower instantaneous power consumption. On the other hand, CMOS logic has a bigger chip size, more latency, and higher power consumption. These results imply that Domino logic is a better option for creating dependable and effective digital circuits.

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